FIG. 1

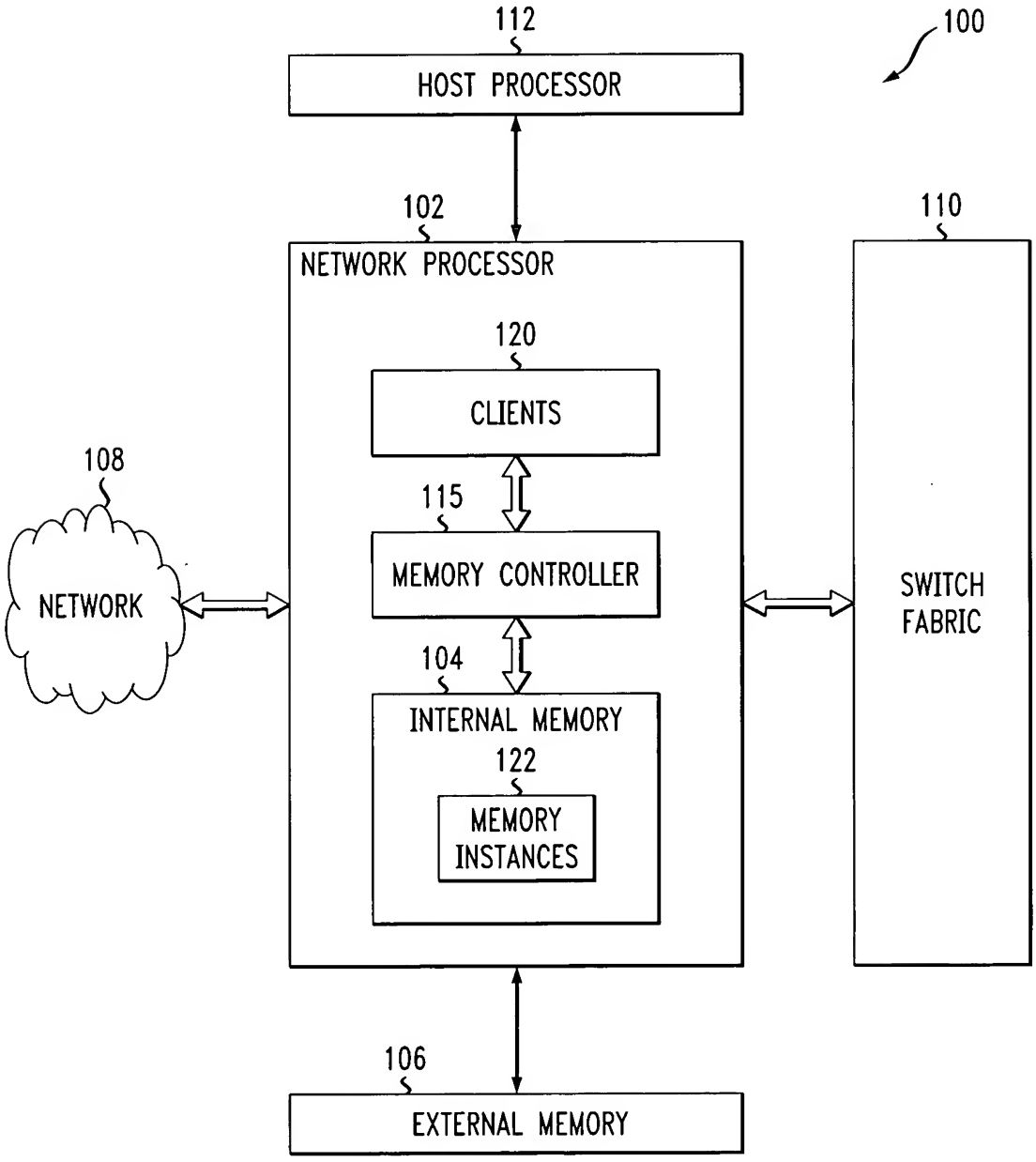

FIG. 2

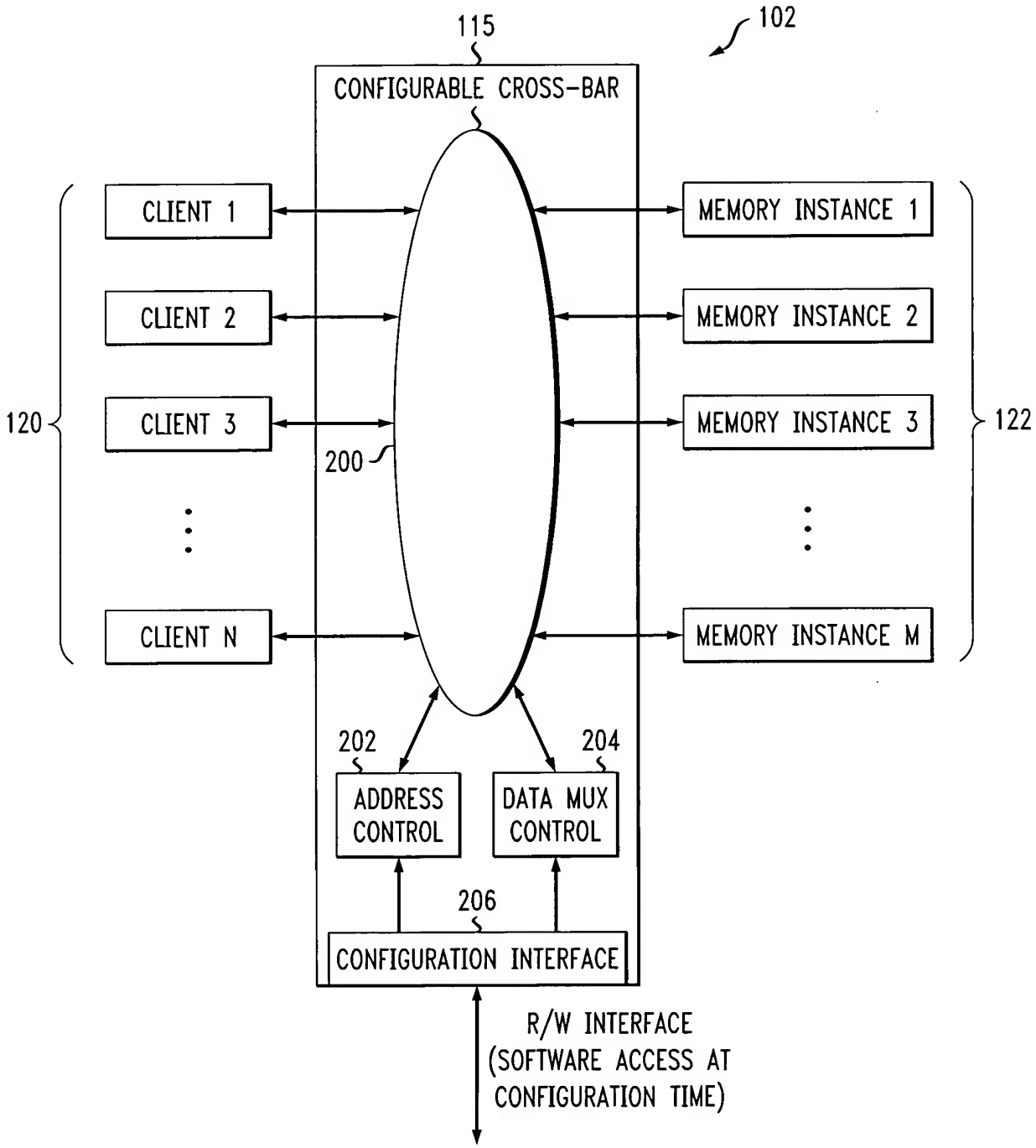

FIG. 3A

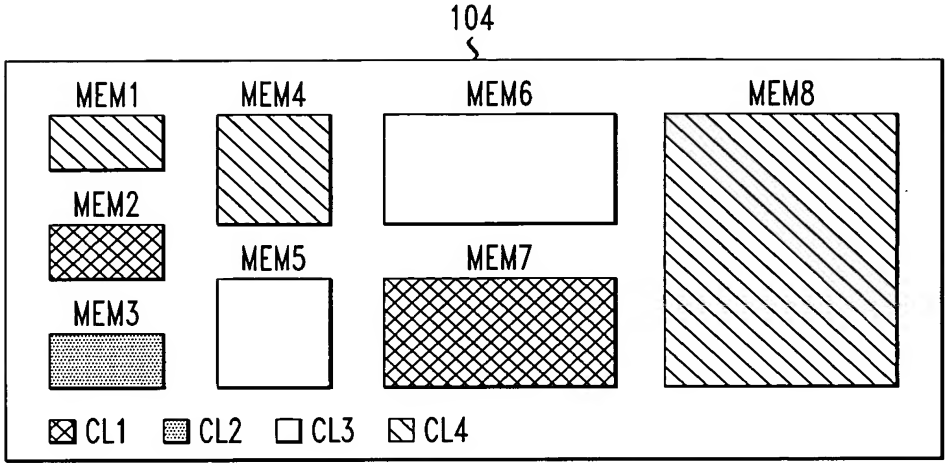

FIG. 3B

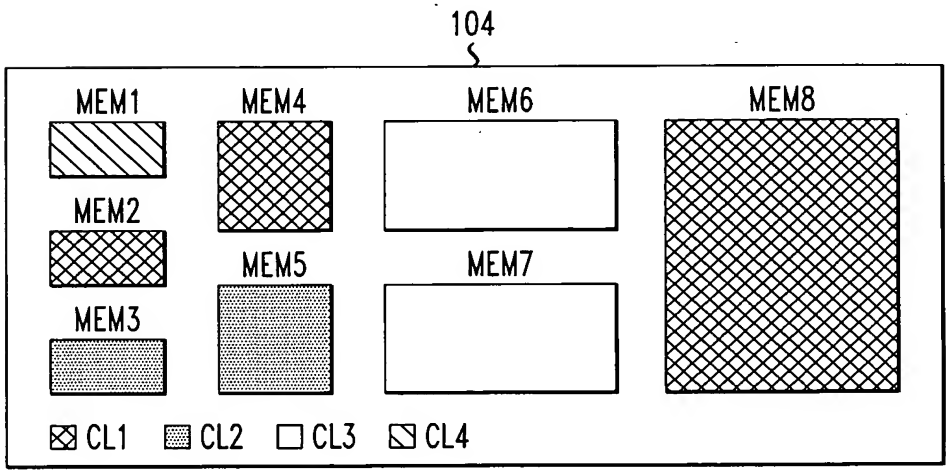

FIG. 4A

MEMORY	CONFIGURED CAPACITY	WORD ADDRESSING RANGE [19:0]		ADDRESS DECODER VALUE [6:0]	ADDRESS MASK BITS [6:0]	RELEVANT BITS
MEM1	1MB	00000h	3FFFFh	7'b00x_xxxx	7'b001_1111	[19:18]
MEM2	1MB	40000h	7FFFFh	7'b01x_xxxx	7'b001_1111	[19:18]
MEM3	512KB	80000h	9FFFFh	7'b100_xxxx	7'b000_1111	[19:17]
MEM4	512KB	A0000h	BFFFFh	7'b101_xxxx	7'b000_1111	[19:17]
MEM5	256KB	C0000h	CFFFFh	7'b110_0xxx	7'b000_0111	[19:16]
MEM6	128KB	D0000h	D7FFFh	7'b110_10xx	7'b000_0011	[19:15]
MEM7	128KB	D8000h	DFFFFh	7'b110_11xx	7'b000_0011	[19:15]
MEM8	64KB	E0000h	E3FFFh	7'b111_000x	7'b000_0001	[19:14]
MEM9	32KB	E4000h	E5FFFh	7'b111_0010	7'b000_0000	[19:13]

FIG. 4B

MEMORY SIZE	MASK BITS [6:0]
1MB	7'b001_1111
512KB	7'b000_1111
256KB	7'b000_0111
128KB	7'b000_0011
64KB	7'b000_0001
32KB	7'b000_0000

FIG. 4C

No. OF BITS	DESCRIPTION
[6:0]	ADDRESS DECODER VALUE FOR A PARTICULAR INTERNAL MEMORY INSTANCE.
[6:0]	ADDRESS MASK VALUE AS MENTIONED IN THE ABOVE TABLE, DEPENDING ON THE MEMORY INSTANCE SIZE.
[4:0]	MASTER CLIENT FOR THE MEMORY INSTANCE. "00001" FOR CL1..... "10100" FOR CL20.

FIG. 5